

1 1. An input buffer receiver comprising:

2 a buffer input portion for receiving an input signal, said buffer input
3 portion comprising a bias node;

4 a large capacitor coupled between the bias node and a lower
5 supply voltage for providing a coupling ratio between said large
6 capacitor and a parasitic capacitor coupled between said bias
7 node and a ground reference point is approximately equal to a
8 unity value such that a biasing voltage at said biasing node
9 follows said lower supply voltage to minimize effects of a ground
10 noise signal between the lower supply voltage and the ground
11 reference point; and

12 a buffer output portion in communication with the buffer input
13 portion for producing an output signal.

1 2. The input buffer receiver of claim 1, wherein the buffer input portion which
2 receives the input signal further comprises:

3 a first transistor of a first conductivity type having a source node to
4 which the lower supply voltage is applied, a gate node to which
5 a reference voltage is applied, and a drain node at which the
6 biasing voltage is developed ;

7 a second transistor of a second conductivity type having a drain
8 node which is connected to the drain node of the first transistor,
9 and a gate node at which the biasing voltage is developed, and
10 a source node to which an upper supply voltage source is
11 applied;

12 a third transistor of the second conductivity type having a drain
13 node, a gate node at which the biasing voltage is developed,
14 and a source node to which the upper supply voltage source is
15 applied;

16 a fourth transistor of the first conductivity type having a source node
17 to which the lower supply voltage is applied, a gate node to
18 which the input signal is applied, and a drain node which is
19 coupled to the drain of a fourth transistor and to an input node of
20 the buffer output portion.

- 1 3. The input buffer receiver of claim 2, wherein the first and fourth transistors
2 are NMOS transistors, and the second and third transistors are PMOS
3 transistors.
- 1 4. The input buffer receiver of claim 2, wherein the large capacitor is
2 connected between the sources of the first and fourth transistors of the

- 3 buffer input portion and the gate of the second transistor of the buffer input
4 portion.
- 1 5. The input buffer receiver of claim 2, wherein the gate of the second
2 transistor is connected to its drain.
- 1 6. The input buffer receiver of claim 2, wherein the gate of the second
2 transistor is connected to the drain of the first transistor.
- 1 7. The input buffer receiver of claim 2, wherein the gate of the second
2 transistor is connected to the gate of the third transistor.
- 1 8. The input buffer receiver of claim 2, wherein the buffer output portion
2 which produces the output signal comprises: a first inverter connected to
3 the drain of the third transistor and the drain of the fourth transistor.
- 1 9. The input buffer receiver of claim 2, wherein the third transistor and the
2 fourth transistor activate and deactivate almost simultaneously as
3 determined by said input signal to minimize the effects of ground noise on
4 a delay jitter factor of said input buffer.
- 1 10. The input buffer receiver of claim 1, wherein the large capacitor charge
2 couples the bias node of the input buffer receiver to the lower supply

3 voltage of the input buffer receiver and wherein a capacitance value of the
4 large capacitor is selected by the formula:

5
$$\frac{CHC}{Cp + CHC} \approx 1$$

6 where:

7 **CHC** is the capacitance value of the large capacitor,
8 and

9 **Cp** is the capacitance value of the parasitic capacitor.

1 11. The input buffer receiver of claim 1, wherein the capacitance value of the
2 large capacitor is chosen to be very large with respect to a capacitance
3 value of said parasitic capacitor and results in a quicker response time for
4 the output signal.

1 12. An integrated circuit formed on a substrate comprising:
2 an input buffer receiver for receiving an input signal, said input
3 buffer comprising:
4 a buffer input portion for receiving the input signal, said
5 buffer input portion comprising a bias node;

6 a large capacitor coupled between the bias node and a
7 lower supply voltage for providing a coupling ratio
8 between said large capacitor and a parasitic capacitor
9 coupled between said bias node and a ground
10 reference point is approximately equal to a unity value
11 such that a biasing voltage at said biasing node
12 follows said lower supply voltage to minimize effects
13 of a ground noise signal between the lower supply
14 voltage and the ground reference point ; and

15 a buffer output portion in communication with the buffer
16 input portion for producing an output signal.

1 13. The integrated circuit of claim 12, wherein the buffer input portion of the
2 input buffer receiver further comprises:

3 a first transistor of a first conductivity type having a source node to
4 which the lower supply voltage is applied, a gate node to which
5 a reference voltage is applied, and a drain node at which the
6 biasing voltage is developed;

7 a second transistor of a second conductivity type having a drain
8 node which is connected to the drain node of the first transistor,

9 and a gate node at which the biasing voltage is developed, and
10 a source node to which an upper supply voltage source is
11 applied;

12 a third transistor of the second conductivity type having a drain
13 node, a gate node at which the biasing voltage is developed,
14 and a source node to which the upper supply voltage source is
15 applied;

16 a fourth transistor of the first conductivity type having a source node
17 to which the lower supply voltage is applied, a gate node to
18 which an input signal is applied, and a drain node which is
19 connected to the drain of a fourth transistor and to an input node
20 of the buffer output portion.

- 1 14. The integrated circuit of claim 13, wherein the first and fourth transistors
2 are NMOS transistors, and the second and third transistors are PMOS
3 transistors.
- 1 15. The integrated circuit of claim 13, wherein the large capacitor is connected
2 between the sources of the first and fourth transistors of the buffer input
3 portion and the gate of the second transistor of the buffer input portion.

$$\frac{CHC}{C_p + CHC} \approx 1$$

6 where:

7 **CHC** is the capacitance value of the large capacitor,

8 and

9 **Cp** is the capacitance value of the parasitic capacitor.

1 22. The integrated circuit of claim 12, wherein the capacitance value of the
2 large capacitor is chosen to be very large with respect to a capacitance
3 value of said parasitic capacitor and results in a quicker response time for
4 the output signal.

1 23. A method for minimizing effects of ground noise on an input buffer
2 receiver comprising the steps of:

3 forming a buffer input portion for receiving an input signal on a
4 substrate;

5 forming a bias node within said buffer input portion;

6 connecting a lower supply voltage to said buffer input portion;

7 forming a large capacitor coupled between the bias node and the
8 lower supply voltage for providing a coupling ratio between said
9 large capacitor and a parasitic capacitor coupled between said

10 bias node and a ground reference point is approximately equal
11 to a unity value such that a biasing voltage at said biasing node
12 follows said lower supply voltage to minimize effects of [[a]] said
13 ground noise between the lower supply voltage and the ground
14 reference point; and

15 forming a buffer output portion on said substrate in communication
16 with the buffer input portion for producing an output signal.

1 24. The method of claim 23, wherein forming the buffer input portion further
2 comprises the steps of:

3 forming a first transistor of a first conductivity type on said
4 substrate;

5 applying the lower supply voltage to a source node of the first
6 transistor;

7 applying a reference voltage to a gate node of the first transistor;
8 connecting a drain node of the first transistor to develop [[as]] a
9 biasing voltage at said drain node;

10 forming a second transistor of a second conductivity type on said
11 substrate;

12 connecting a drain node of the second transistor to the drain node
13 of the first transistor;
14 connecting a gate node of the second transistor to the drain node of
15 the first transistor for developing the biasing voltage; and
16 connecting a source node of the second transistor to an upper
17 supply voltage;
18 forming a third transistor of the second conductivity type on said
19 substrate;
20 connecting a gate node of the third transistor to the drain node of
21 the first transistor for developing the biasing voltage;
22 connecting a source node of the third transistor to the upper supply
23 voltage source;
24 forming a fourth transistor of the first conductivity type on said
25 substrate;
26 connecting a source node of the fourth transistor to the lower
27 supply voltage;

28 connecting a gate node of the fourth transistor to receive an input
29 signal; and

30 connecting a drain node of the fourth transistor to a drain node of
31 the third transistor and to an input node of the buffer output
32 portion.

1 25. The method of claim 24, wherein the first and fourth transistors are NMOS
2 transistors, and the second and third transistors are PMOS transistors.

1 26. The method of claim 24, wherein forming the large capacitor comprises
2 the step of:

3 connecting said large capacitor between the sources of the first and
4 fourth transistors of the buffer input portion and the gate of the
5 second transistor of the buffer input portion.

1 27. The method of claim 24, wherein forming the buffer input portion further
2 comprises the steps of:

3 connecting the gate of the second transistor to its drain.

1 28. The method of claim 24, wherein forming the buffer input portion further
2 comprises the steps of:

3 connecting the gate of the second transistor to the gate of the third
4 transistor.

1 29. The method of claim 24, wherein forming the buffer output portion which
2 produces the output signal comprises the step of:

3 forming a first inverter on said substrate; and

4 connecting an input of said first inverter to the drain of the third
5 transistor and the drain of the fourth transistor.

1 30. The method of claim 24, wherein the third transistor and the fourth
2 transistor activate and deactivate almost simultaneously as determined by
3 said input signal to minimize the effects of ground noise on a delay jitter
4 factor of said input buffer.

1 31. The method of claim 23, wherein the large capacitor charge couples the
2 bias node of the input buffer receiver to the lower supply voltage of the
3 input buffer receiver and wherein a capacitance value of the large
4 capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

6 where:

7 **CHC** is the capacitance value of the large capacitor,

8 and

9 **C_p** is the capacitance value of the parasitic capacitor.

1 32. The method of claim 23, wherein the capacitance value of the large
2 capacitor is chosen to be very large with respect to a capacitance value of
3 said parasitic capacitor and results in a quicker response time for the
4 output signal.

1 33. An apparatus for minimizing effects of ground noise on an input buffer
2 receiver, said apparatus comprising:

3 means for forming a buffer input portion for receiving an input signal
4 on a substrate;

5 means for forming a bias node within said buffer input portion;

6 means for connecting said a lower supply voltage to said buffer
7 input portion;

8 means for forming a large capacitor between the bias node and the
9 lower supply voltage for providing a coupling ratio between said
10 large capacitor and a parasitic capacitor coupled between said
11 bias node and a ground reference point is approximately equal

12 to a unity value such that a biasing voltage at said biasing node
13 follows said lower supply voltage to minimize effects of [[a]] said
14 ground noise between the lower supply voltage and the ground
15 reference point; and

16 means for forming a buffer output portion on said substrate in
17 communication with the buffer input portion for producing an
18 output signal.

1 34. The apparatus of claim 33, wherein forming the buffer input portion further
2 comprises:

3 means for forming a first transistor of a first conductivity type on
4 said substrate;

5 means for applying the lower supply voltage to a source node of the
6 first transistor;

7 means for applying a reference voltage to a gate node of the first
8 transistor;

9 means for connecting a drain node of the first transistor to develop
10 as biasing voltage at said drain node;

11 means for forming a second transistor of a second conductivity type
12 on said substrate;

13 means for connecting a drain node of the second transistor to the
14 drain node of the first transistor;

15 means for connecting a gate node of the second transistor to the
16 drain node of the first transistor for developing the biasing
17 voltage; and

18 means for connecting a source node of the second transistor to an
19 upper supply voltage;

20 means for forming a third transistor of the second conductivity type
21 on said substrate;

22 means for connecting a gate node of the third transistor to the drain
23 node of the first transistor for developing the biasing voltage;

24 means for connecting a source node of the third transistor to the
25 upper supply voltage source;

26 means for forming a fourth transistor of the first conductivity type on
27 said substrate;

28 means for connecting a source node of the fourth transistor to the
29 lower supply voltage;

30 means for connecting a gate node of the fourth transistor to receive
31 [[an]] said input signal; and

32 connecting a drain node of the fourth transistor to a drain node of
33 the third transistor and to an input of the buffer output portion.

- 1 35. The apparatus of claim 34, wherein the first and fourth transistors are
2 NMOS transistors, and the second and third transistors are PMOS
3 transistors.

- 1 36. The apparatus of claim 34, wherein means for forming the large capacitor
2 comprises:

3 means for connecting said large capacitor between the sources of
4 the first and fourth transistors of the buffer input portion and the
5 gate of the second transistor of the buffer input portion.

- 1 37. The apparatus of claim 34, wherein means for forming the buffer input
2 portion further comprises:

3 means for connecting the gate of the second transistor to its drain.

- 1 38. The apparatus of claim 34, wherein means for forming the buffer input
- 2 portion further comprises the steps of:
 - 3 means for connecting the gate of the second transistor to the gate
 - 4 of the third transistor.
- 1 39. The apparatus of claim 34, wherein means for forming the buffer output
- 2 portion which produces said output signal comprises:
 - 3 means for forming a first inverter on said substrate; and
 - 4 means for connecting an input of said first inverter to the drain of
 - 5 the third transistor and the drain of the fourth transistor.
- 1 40. The apparatus of claim 34, wherein the third transistor and the fourth
- 2 transistor activate and deactivate almost simultaneously as determined by
- 3 said input signal to minimize the effects of ground noise on a delay jitter
- 4 factor of said input buffer.
- 1 41. The apparatus of claim 33, wherein the large capacitor charge couples the
- 2 bias node of the input buffer receiver to the lower supply voltage of the
- 3 input buffer receiver and wherein a capacitance value of the large
- 4 capacitor is selected by the formula:

5
$$\frac{CHC}{Cp + CHC} \approx 1$$

6 where:

7 **CHC** is the capacitance value of the large capacitor

8 **CHC**, and

9 **Cp** is the capacitance value of the parasitic capacitor

10 **Cp**.

42. The apparatus of claim 33, wherein the capacitance value of the large capacitor is chosen to be very large with respect to a capacitance value of said parasitic capacitor and results in a quicker response time for the output signal.